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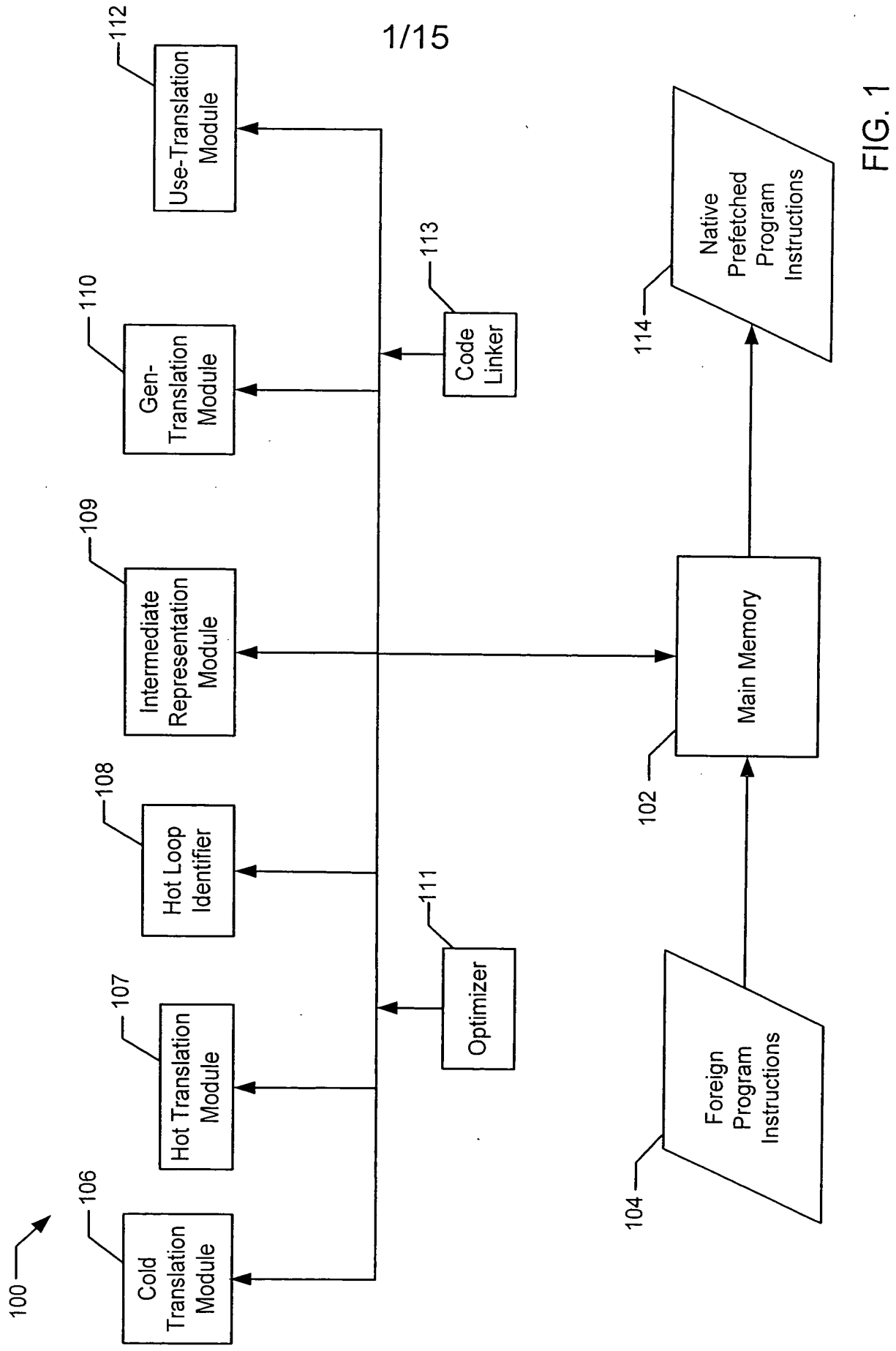
100
Cold Translation Module
106
Hot Translation Module
107
Hot Loop Identifier
108
Intermediate Representation Module
109
Gen-Translation Module
110
Use-Translation Module
112
Optimizer
111
Code Linker
113
Main Memory
102
Foreign Program Instructions
104
Native Prefetched Program Instructions
114

FIG. 1

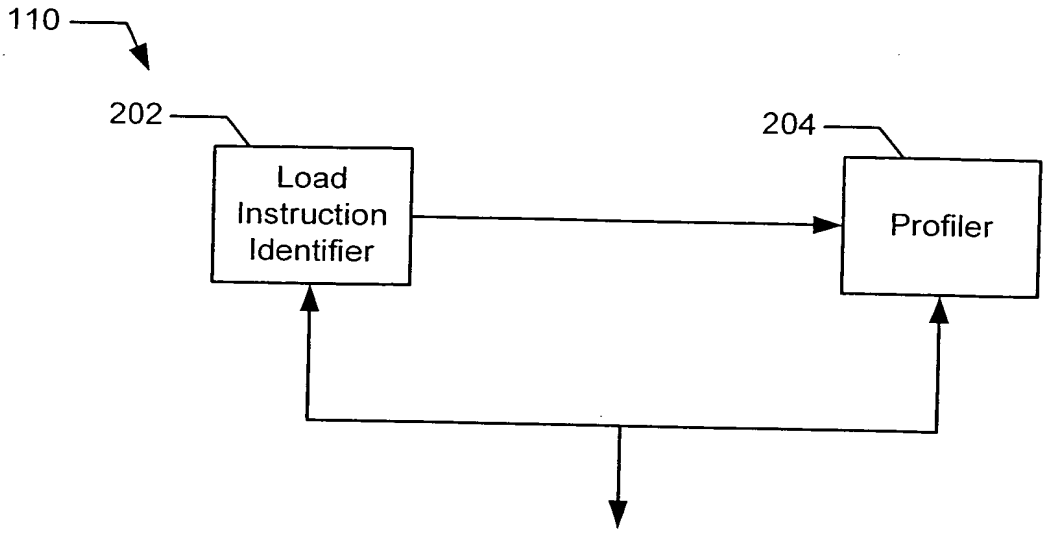
110
202
Load Instruction Identifier
204
Profiler

FIG. 2

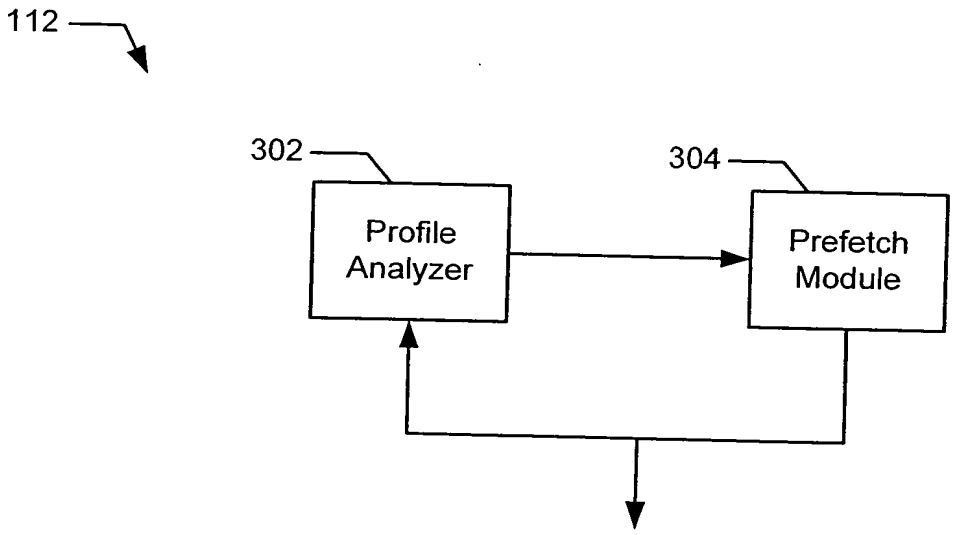
112
302
Profile Analyzer
304
Prefetch Module

FIG. 3

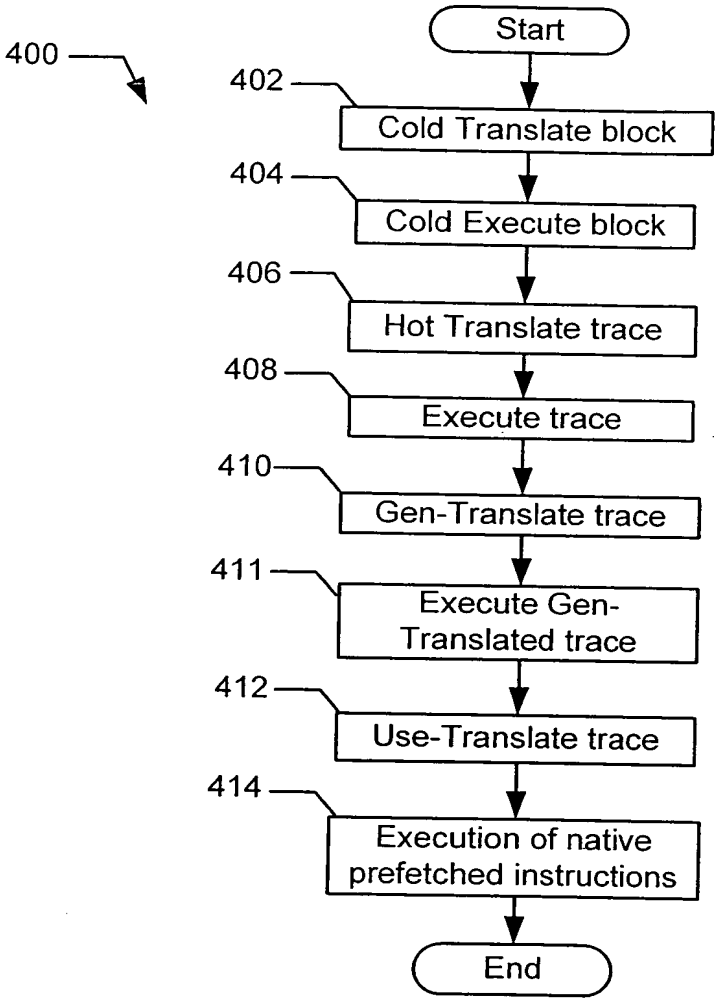
400
Start
402
Cold Translate block
404
Cold Execute block
406
Hot Translate trace
408
Execute trace
410
Gen-Translate trace
411
Execute Gen-Translated trace
412
Use-Translate trace
414
Execution of native prefetched instructions
End

FIG. 4

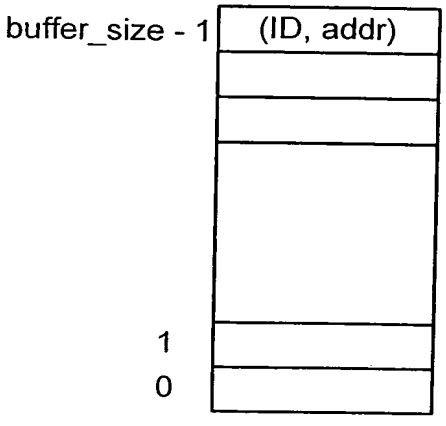
buffer_size - 1
(ID, addr)
1
0

FIG. 15

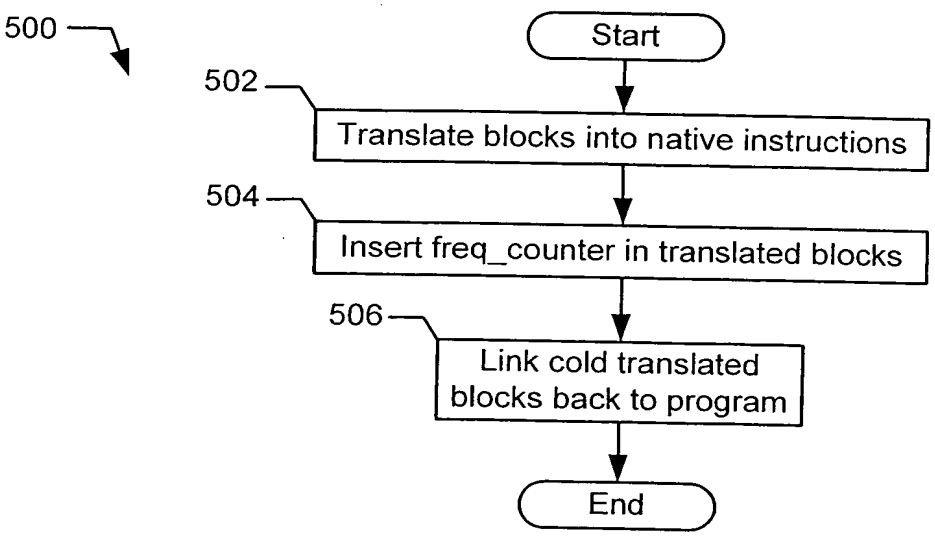
500
Start
502
Translate blocks into native instructions
504
Insert freq_counter in translated blocks
506
Link cold translated blocks back to program
End

FIG. 5

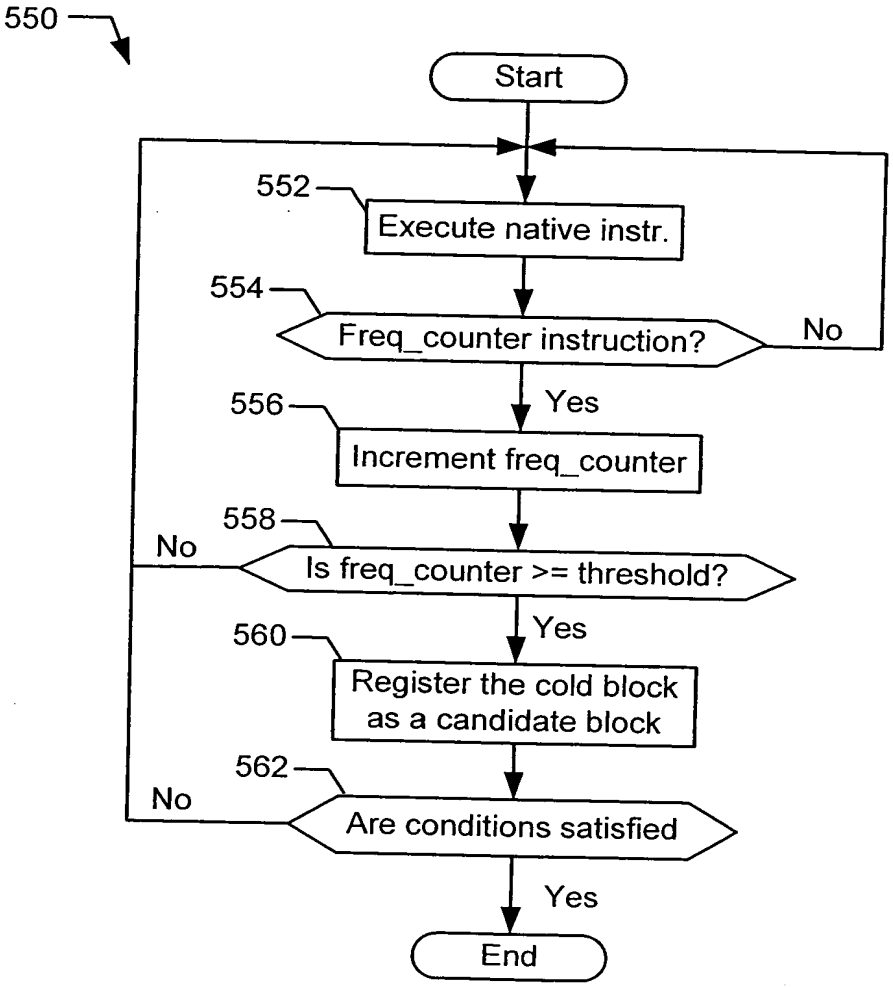
550
Start
552
Execute native instr.
554
Freq_counter instruction?
No
Yes
556
Increment freq_counter
558
No
Is freq_counter >= threshold?
Yes
560
Register the cold block as a candidate block
562
No
Are conditions satisfied
Yes
End

FIG. 6

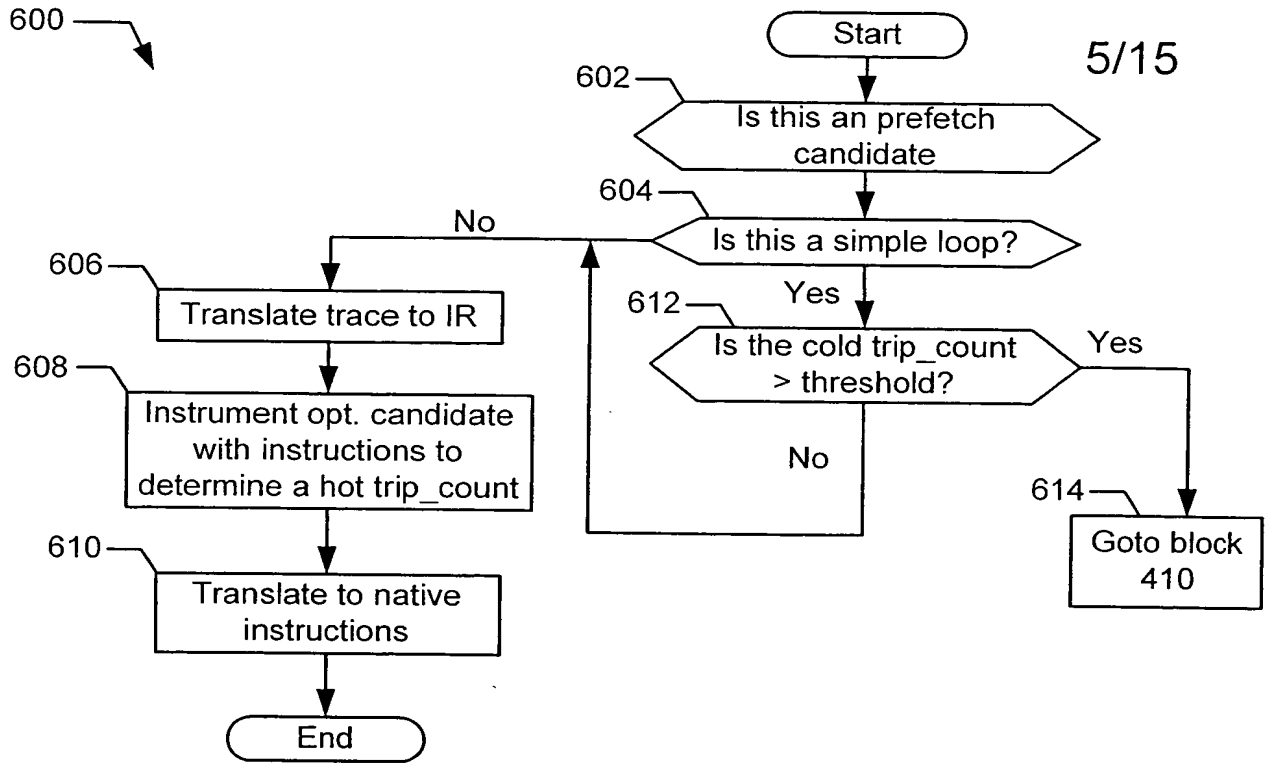
600
Start
602
Is this an prefetch candidate
604
Is this a simple loop?
No
Yes
606
Translate trace to IR
608
Instrument opt. candidate with instructions to determine a hot trip_count
610
Translate to native instructions
End
612
Is the cold trip_count > threshold?
Yes
No
614
Goto block 410

FIG. 7

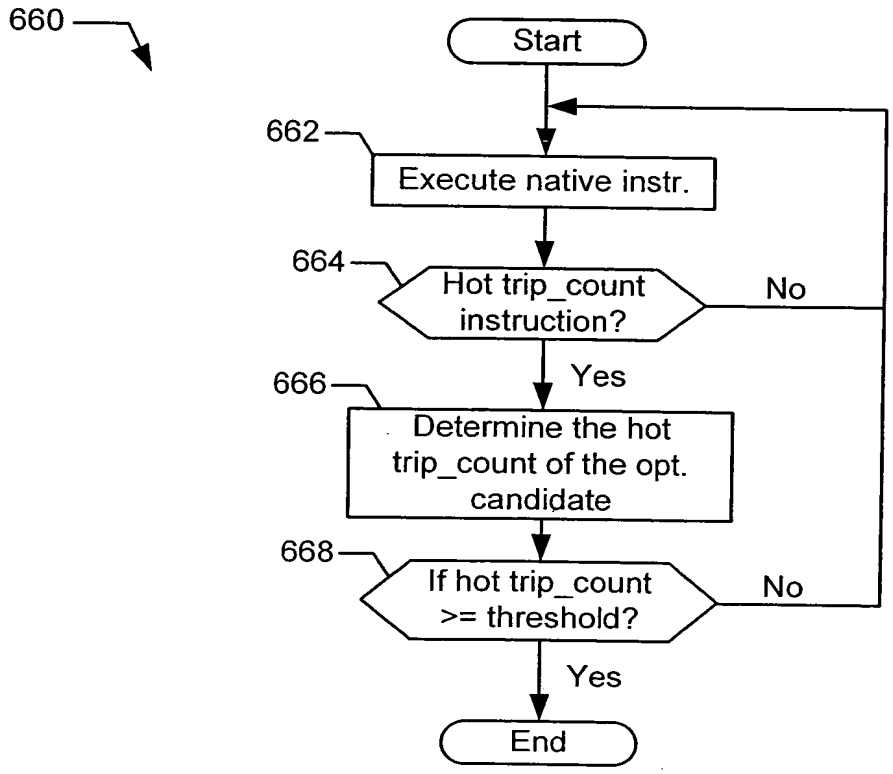
660
Start
662
Execute native instr.
664
Hot trip_count instruction?
No
Yes
666
Determine the hot trip_count of the opt. candidate
668
If hot trip_count >= threshold?
No
Yes
End

FIG. 9

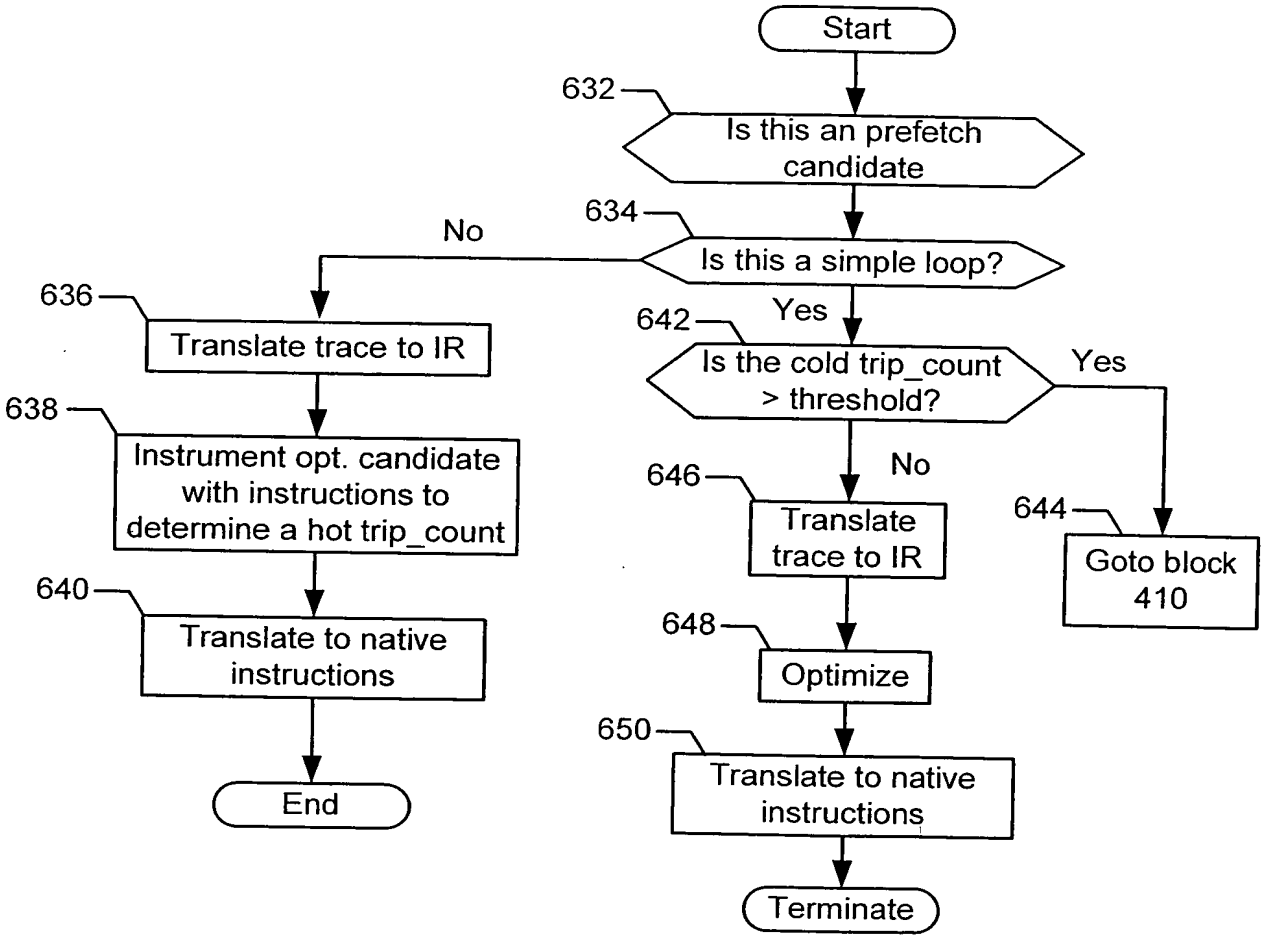
630
Start
632
Is this an prefetch candidate
634
Is this a simple loop?
No
Yes
636
Translate trace to IR
638
Instrument opt. candidate with instructions to determine a hot trip_count
640
Translate to native instructions
End
642
Is the cold trip_count > threshold?
Yes
No
644
Goto block 410
646
Translate trace to IR
648
Optimize
650
Translate to native instructions
Terminate

FIG. 8

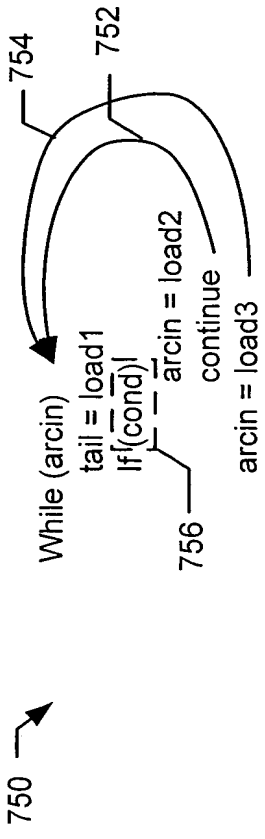

FIG. 10

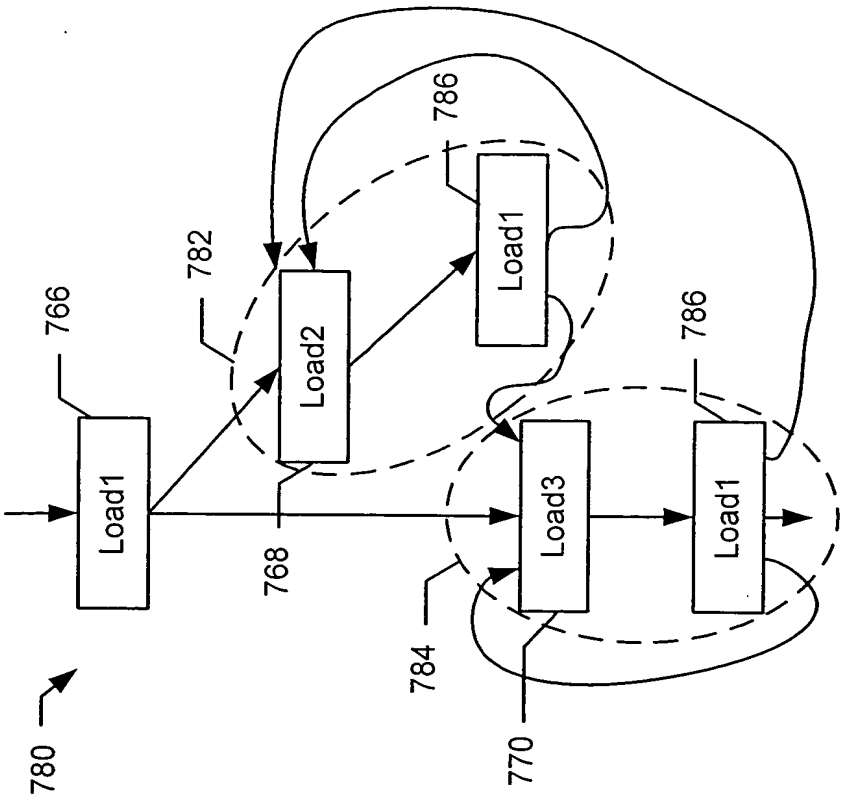

FIG. 12

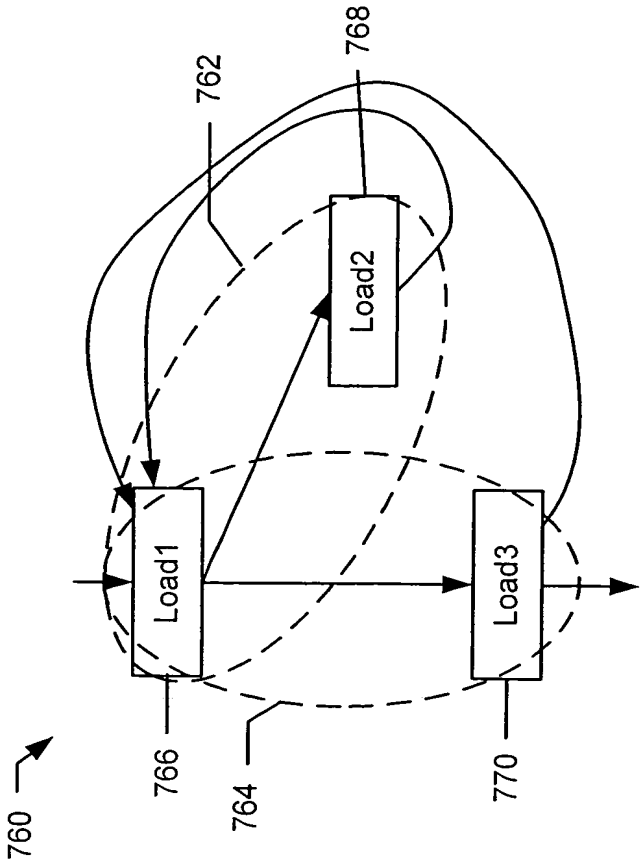

FIG. 11

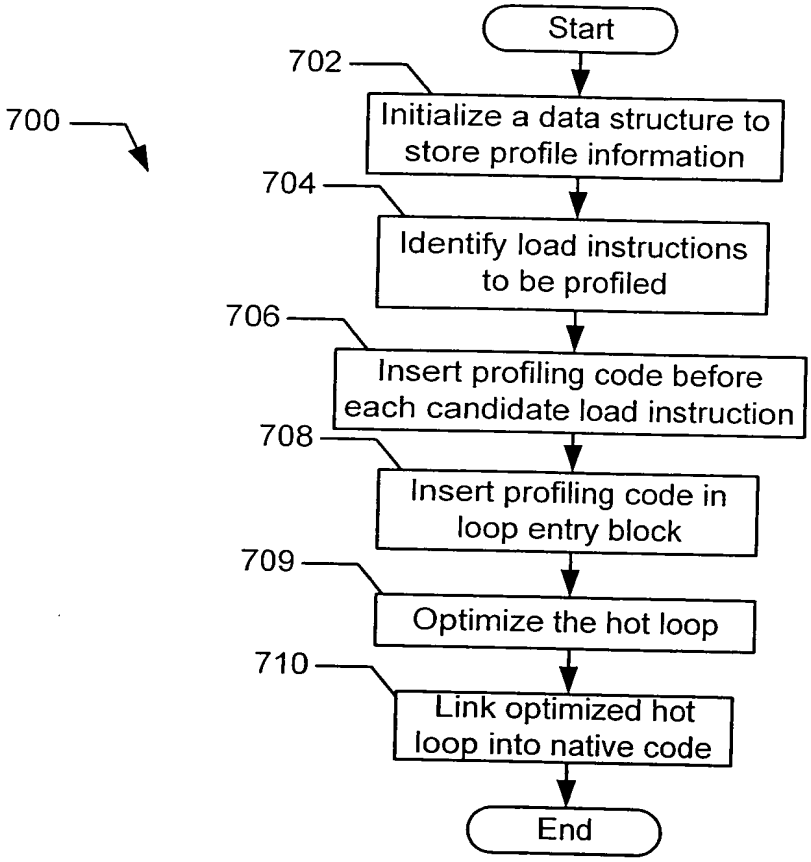
700
Start
702
Initialize a data structure to store profile information
704
Identify load instructions to be profiled
706
Insert profiling code before each candidate load instruction
708
Insert profiling code in loop entry block
709
Optimize the hot loop
710
Link optimized hot loop into native code
End

FIG. 13

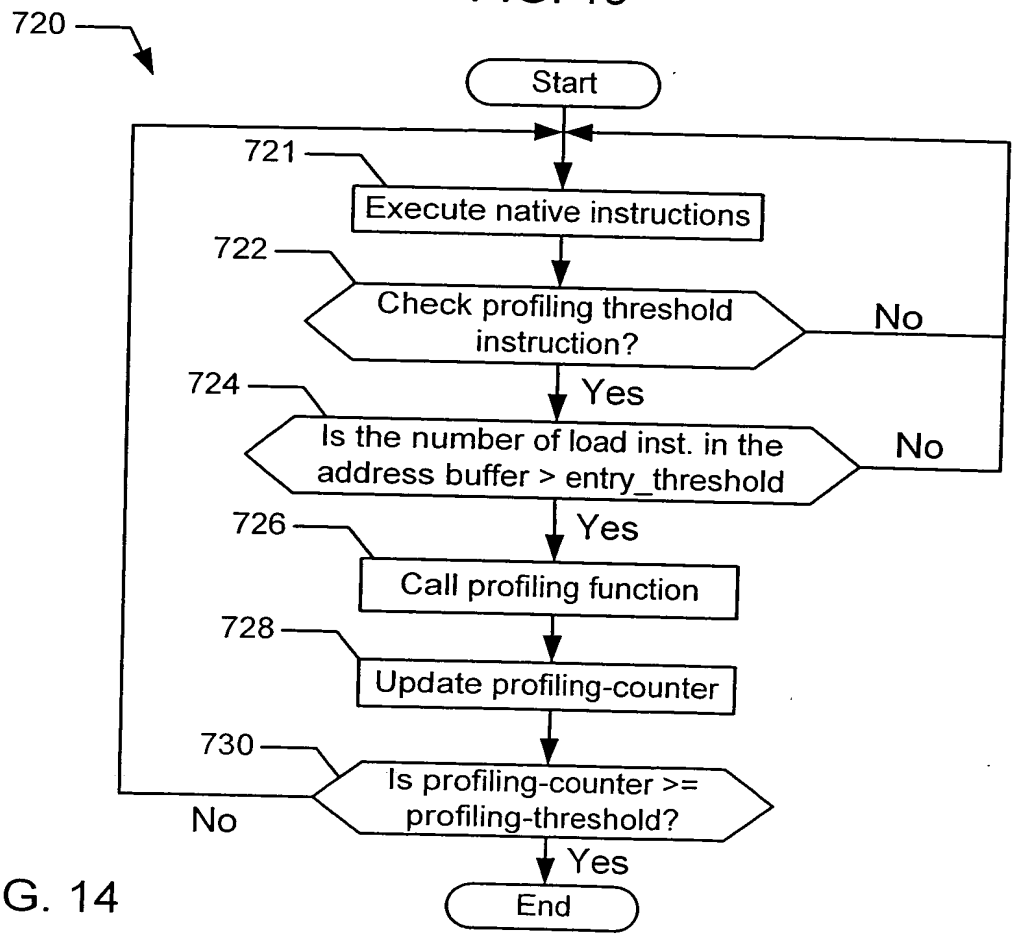
720
Start
721
Execute native instructions
722
Check profiling threshold instruction?
No
Yes
724
Is the number of load inst. in the address buffer > entry_threshold
No
Yes
726
Call profiling function
728
Update profiling-counter
730
Is profiling-counter >= profiling-threshold?
No
Yes
End

FIG. 14

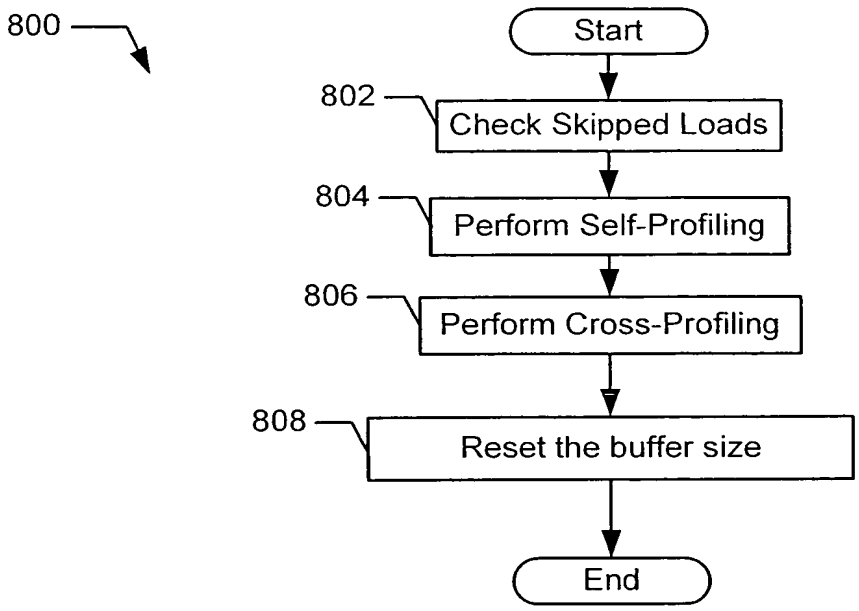
800
Start
802
Check Skipped Loads
804
Perform Self-Profiling
806
Perform Cross-Profiling
808
Reset the buffer size
End

FIG. 16

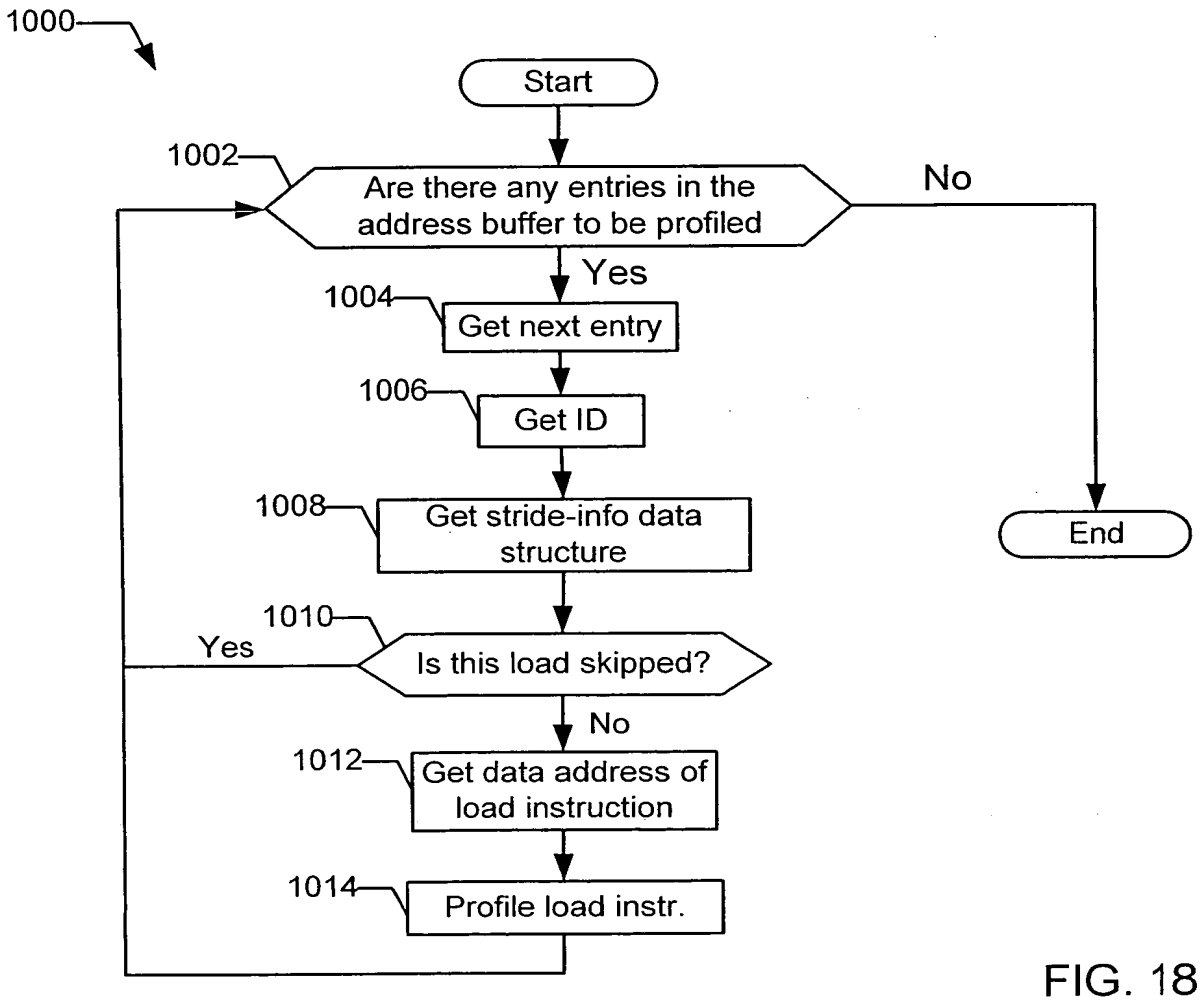
1000
Start
1002
Are there any entries in the address buffer to be profiled
No
Yes
1004
Get next entry
1006
Get ID
1008
Get stride-info data structure
End
1010
Yes
Is this load skipped?
No
1012
Get data address of load instruction
1014
Profile load instr.

FIG. 18

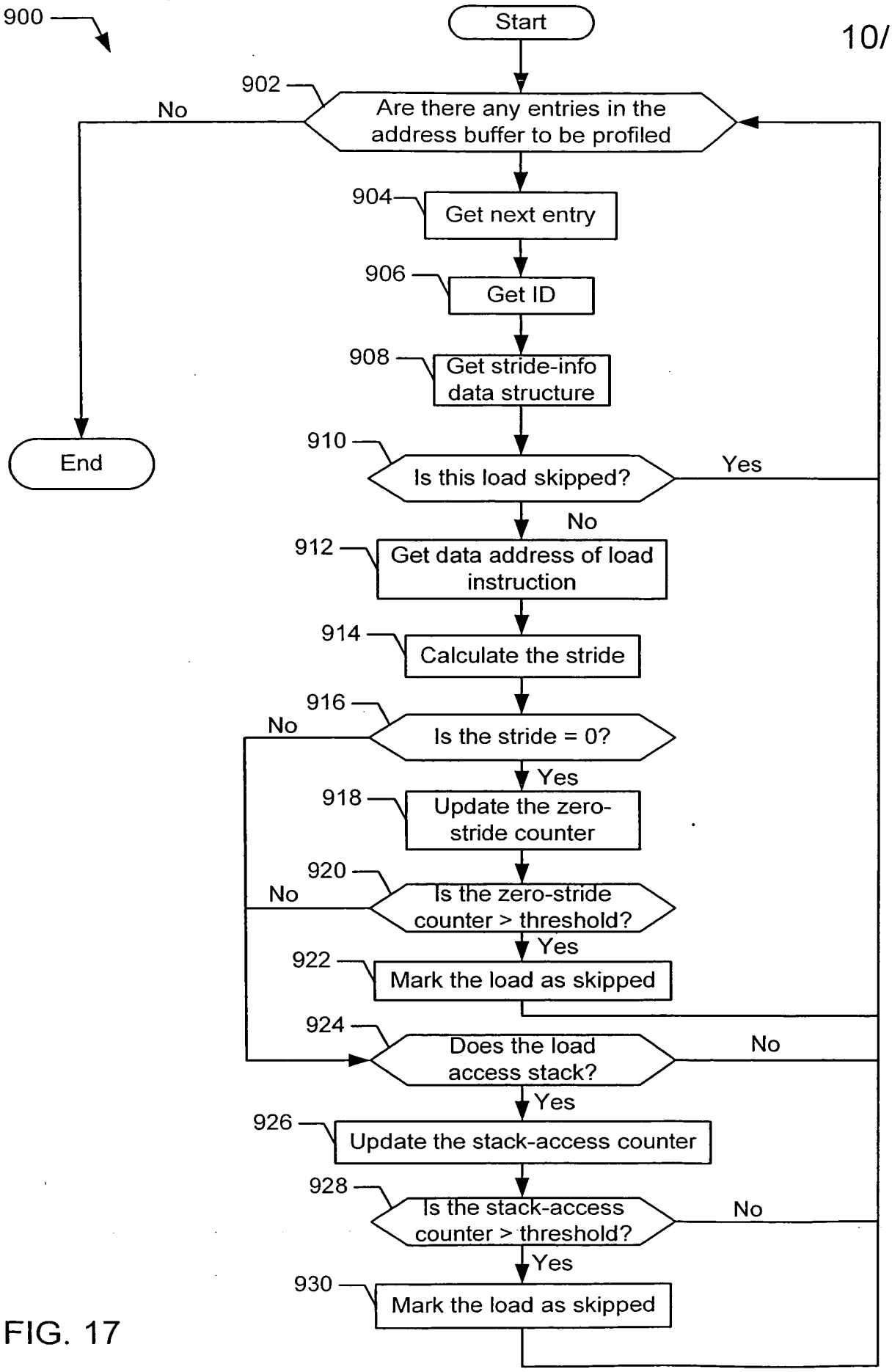
900
Start
902
Are there any entries in the address buffer to be profiled
No
End
904
Get next entry
906
Get ID
908
Get stride-info data structure
910
Is this load skipped?
Yes
No
912
Get data address of load instruction
914
Calculate the stride
916
Is the stride = 0?
No
Yes
918
Update the zero-stride counter
920
Is the zero-stride counter > threshold?
No
Yes
922
Mark the load as skipped
924
Does the load access stack?
No
Yes
926
Update the stack-access counter
928
Is the stack-access counter > threshold?
No
Yes
930
Mark the load as skipped

FIG. 17

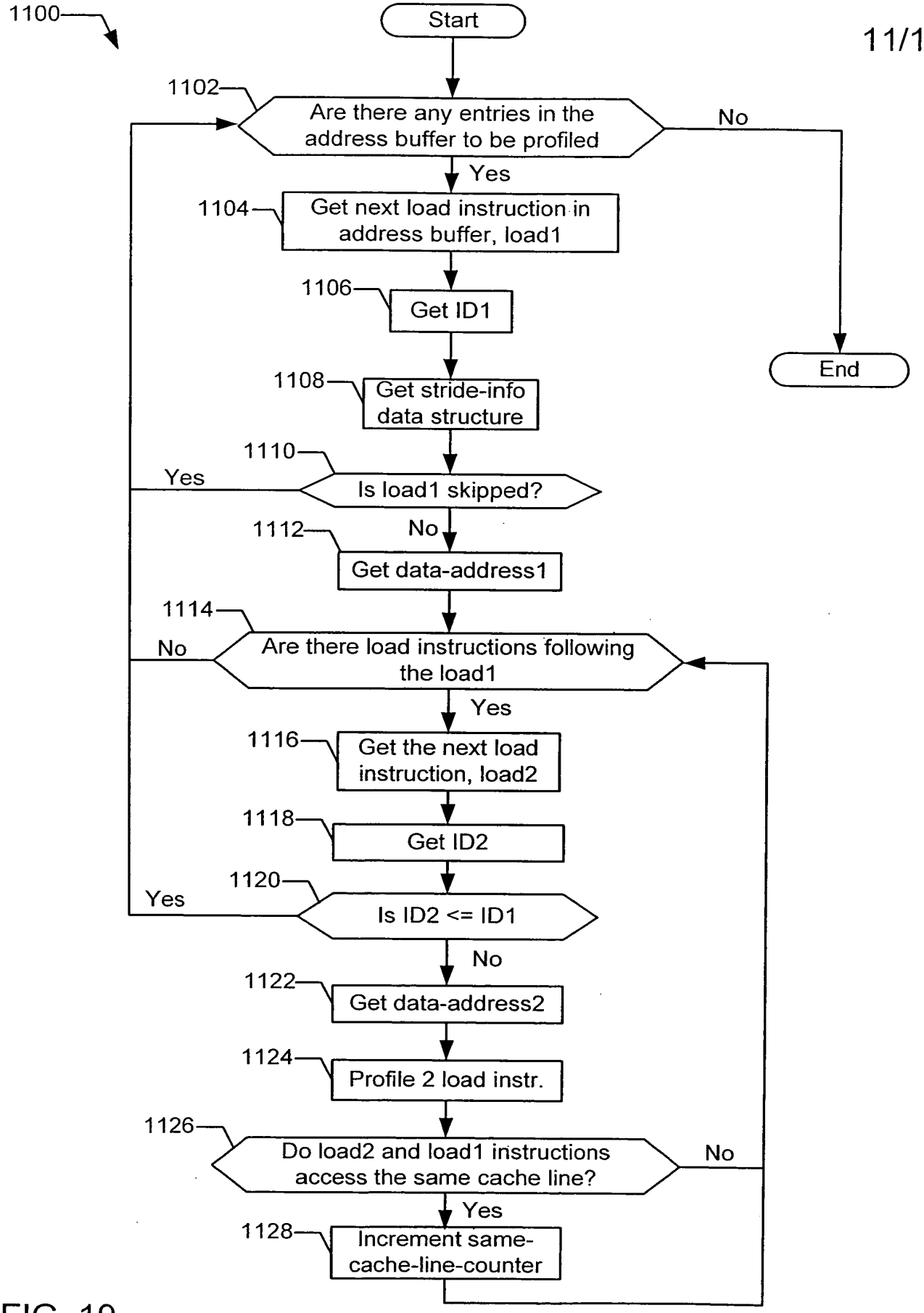
1100
Start
1102
Are there any entries in the address buffer to be profiled
No
Yes
1104
Get next load instruction in address buffer, load1
1106
Get ID1
End
1108
Get stride-info data structure
1110
Yes
Is load1 skipped?
No
1112
Get data-address1
1114
No
Are there load instructions following the load1
Yes
1116
Get the next load instruction, load2
1118
Get ID2
1120
Yes
Is ID2 <= ID1
No
1122
Get data-address2
1124
Profile 2 load instr.
1126
Do load2 and load1 instructions access the same cache line?
No
Yes
1128
Increment same-cache-line-counter

FIG. 19

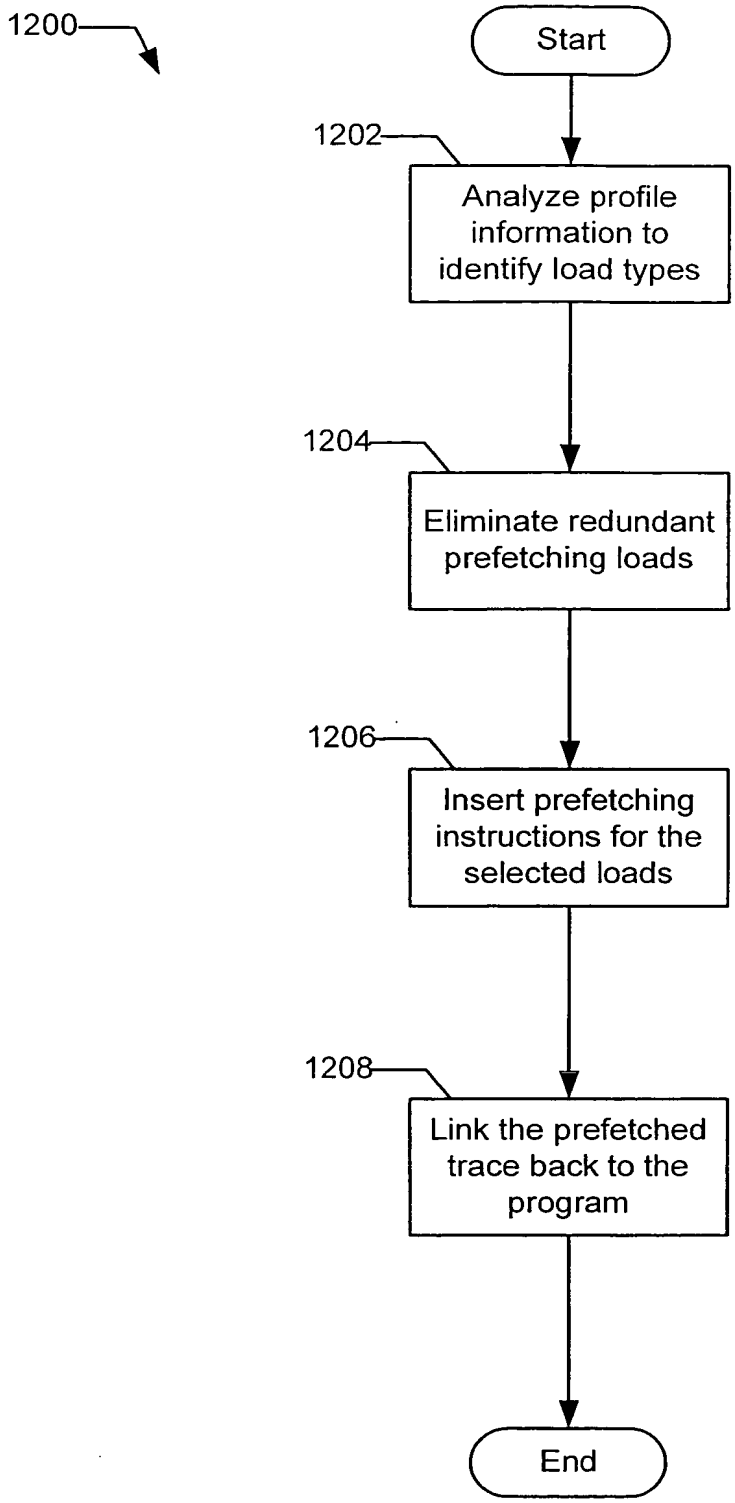
1200
Start
1202
Analyze profile information to identify load types
1204
Eliminate redundant prefetching loads
1206
Insert prefetching instructions for the selected loads
1208
Link the prefetched trace back to the program
End

FIG. 20

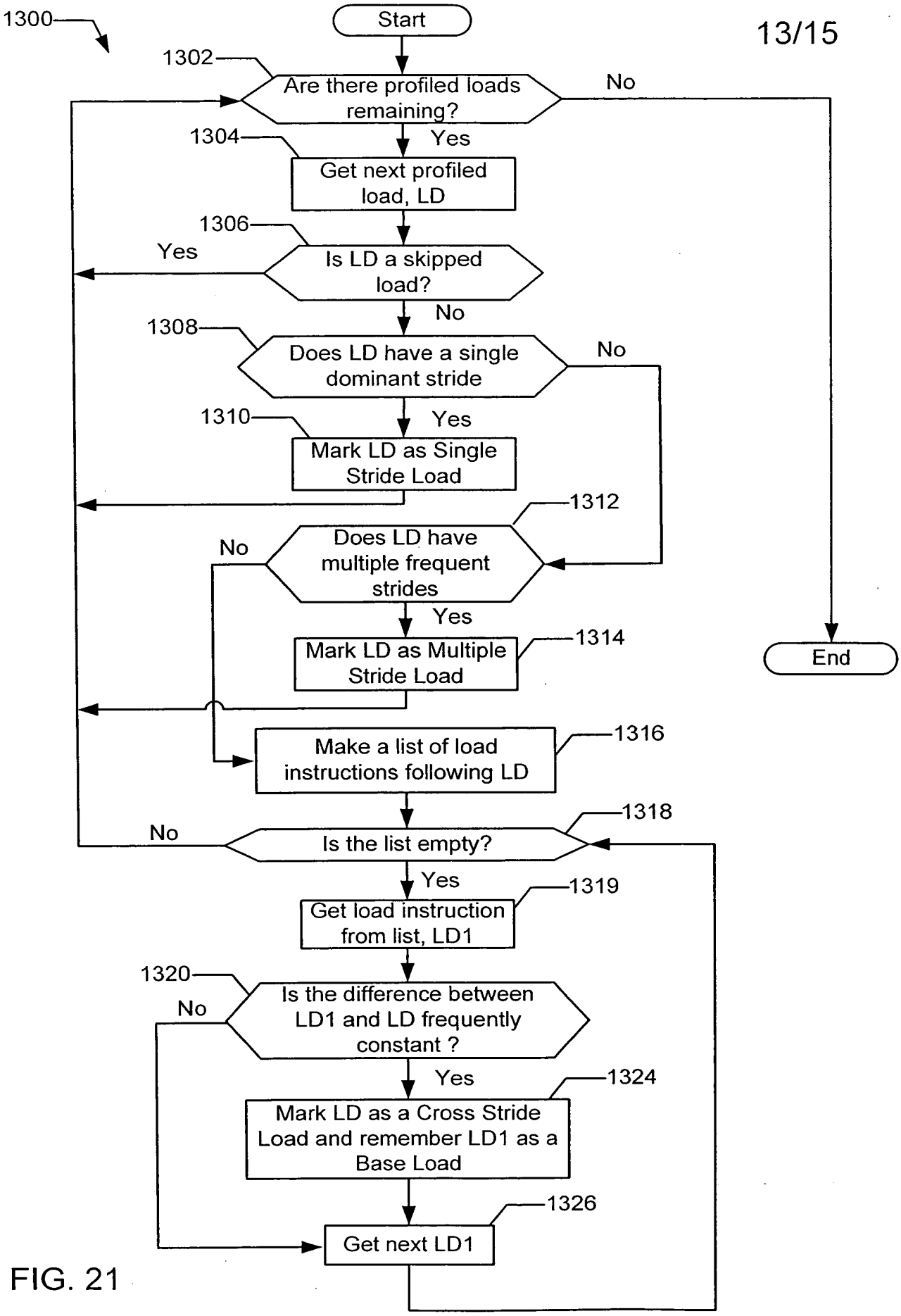
1300
Start
1302
Are there profiled loads remaining?
No
Yes
1304
Get next profiled load, LD
1306
Is LD a skipped load?
Yes
No
1308
Does LD have a single dominant stride
No
Yes
1310
Mark LD as Single Stride Load
1312
Does LD have multiple frequent strides
No
Yes
1314
Mark LD as Multiple Stride Load
End
1316
Make a list of load instructions following LD
1318
Is the list empty?
No
Yes
1319
Get load instruction from list, LD1
1320
Is the difference between LD1 and LD frequently constant ?
No
Yes
1324
Mark LD as a Cross Stride Load and remember LD1 as a Base Load
1326
Get next LD1

FIG. 21

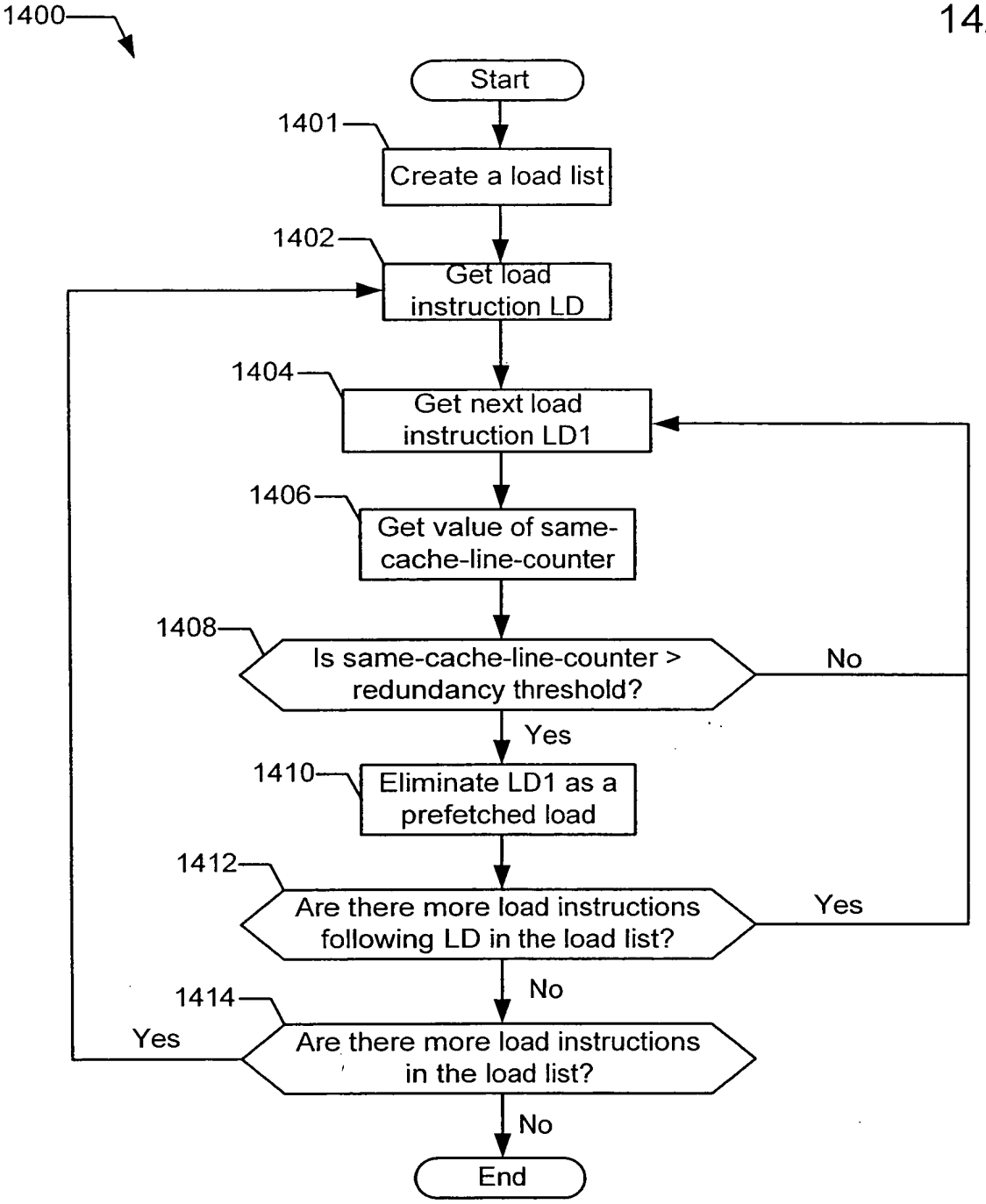
1400
Start
1401
Create a load list
1402
Get load instruction LD
1404
Get next load instruction LD1
1406
Get value of same-cache-line-counter
1408
Is same-cache-line-counter > redundancy threshold?
No
Yes
1410
Eliminate LD1 as a prefetched load
1412
Are there more load instructions following LD in the load list?
Yes
No
1414
Are there more load instructions in the load list?
Yes
No
End

FIG. 22

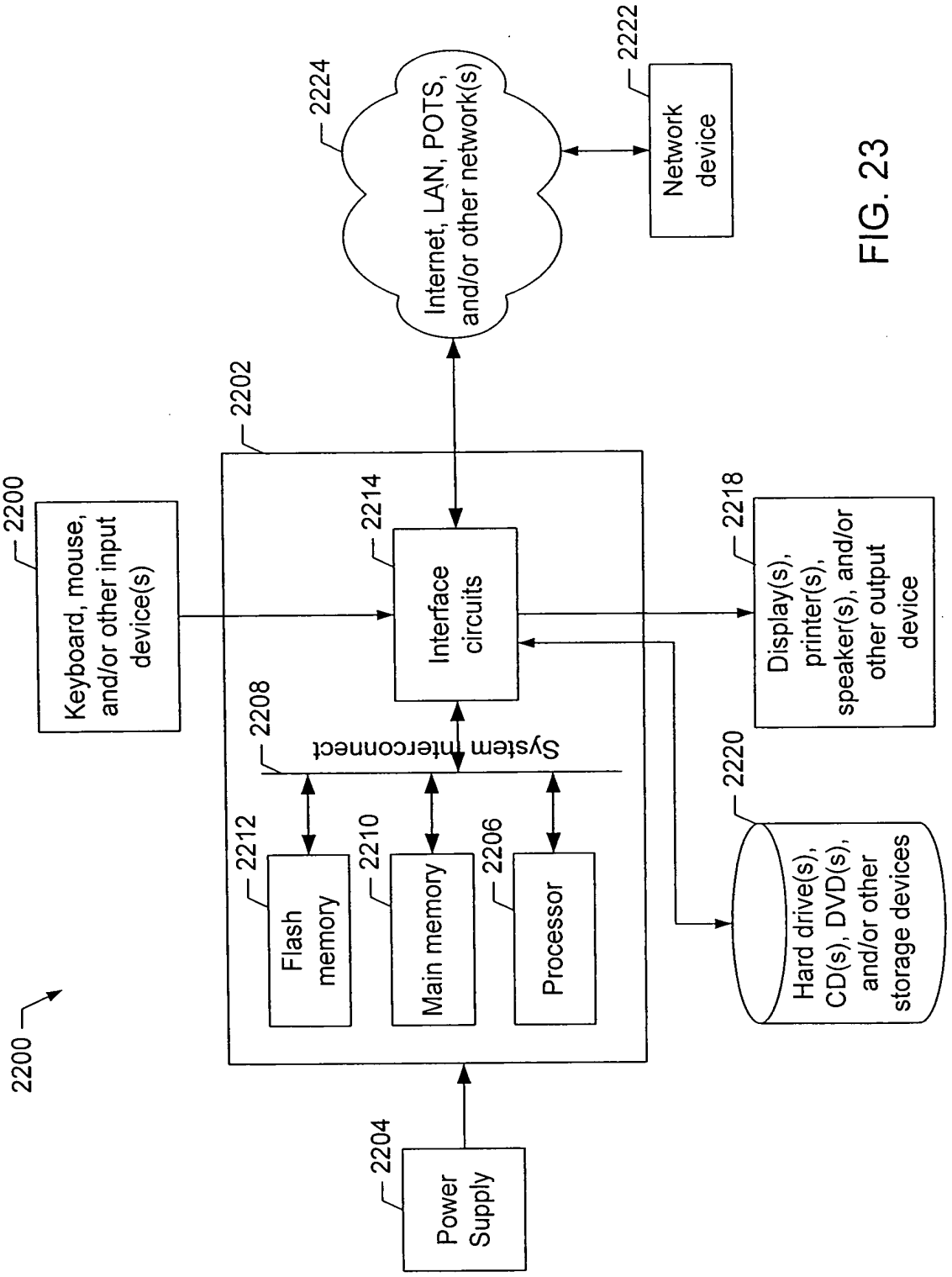
2200
2202
2204
Power Supply
2206
Processor
2208
System Interconnect
2210
Main memory
2212
Flash memory
2214
Interface circuits
2218
Display(s), printer(s), speaker(s), and/or other output device
2220
Hard drive(s), CD(s), DVD(s), and/or other storage devices
2222
Network device
2224
Internet, LAN, POTS, and/or other network(s)
2200
Keyboard, mouse, and/or other input device(s)

FIG. 23